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NOTE:
Signatures enclosed in parentheses should be checked only after all others are correct. Signatures followed by * are pulsed.

Z Intensity and Blanking

R-G-B Output

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Gravitar™ PCB Schematic Diagram

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SP-206 Sheet 7B
1st printing
Adjusting X- and Y-Axis Video Potentiometers

If you replace the main Gravitar PCB or the display, you may have to make the following adjustments:

1. Enter self-test and advance to diagonal crosshatch pattern (Screen 2).
2. Centering Pots: Adjust X CENTER (R189) and Y CENTER (R212) so that the crosshatch pattern is located at the middle of the screen.
3. Size Pots: Adjust XSIZE (R192) and YSIZE (R213) so that the crosshatch pattern exactly covers the whole visible screen.
4. Linearity Pots: Adjust XLIN (R187) and YLIN (R210) so that the diagonal lines are straight. Since the LIN pots change the size of the displayed picture on the screen, you may have to readjust the SIZE pots in order to get the correct adjustment.
5. Bipolar Pots: Advance to the self-test raster pattern (Screen 4). Adjust XBIP (R99) and YBIP (R100) for a 1-inch high horizontal raster in the center of the screen. Be sure the raster ends are square with the sides of the outer rectangle.
Descriptions of Gravitar PCB Signal Names

A10, A13-A15
Address bits on Microprocessor Address Bus lines A10 and A13-A15 are generated by Microprocessor C2. Bits on lines A13-A15, together with those on A11/A12, are the input bits to Address Decoder R112 and R112 is exclusive-Orred with BANK SEL by gate B6 to produce the A10 input bit for Random-Access Memory N1/P1.

A80-A87
Address bits on Buffered Microprocessor Address Bus lines A80-A87 are software-generated by Microprocessor C2 and buffered by Microprocessor C6. Bits on lines A80-A87 are exclusive-Orred with BANK SEL by gate B5 to produce the A80 input bit for Random-Access Memory N1/P1.

A68-A69 are the select input signals for Address Decoder P3.

A11/A12 and A13-A15 are the input bits for Address Decoder R111 and R112.

A8-A80 are control signals to custom audio chips B3 and C123 in the Option Switch Input and Audio Output circuit.

B24 are the input signals to latch P2 in the High-Score Table circuit where they are used to produce the A11 address input for EAROM M2.

B13
B13 is from B13, inverted by J3, and applied to Vector Ad- dress Selector M6. When VOFF is low, B13 and A12 select the specific Memory Read-Only Memory.

AM0-AM13
Address bits on Multiplexed Address Bus lines AM0-AM13 are software-generated by Vector Address Selectors K8, L0, M8, and N8. When VOFF is low, the Multiplexed Address Bus is from Buffered Microprocessor Address Bus A80 through A122 and A132. When VOFF is high, AM0-AM12 is from Vector Generator Address Bus lines AVG0-AVG13. Signals AM0-AM13 are the input address signals to Vector Read-Only Memory LMT, WMT, PTSD, PTSD and to Vector Random-Access Memory K7. In addition, AM11-AM13 are the select input signals for multiplexers N3 and R3 of the State Machine circuit.

AUD 1AUD 2
The Audio 1 and Audio 2 signals are game PCB output signals that are generated by custom audio chips B3 and C123 of the Option Switch Input and Audio Output circuit. AUD 1 is the inverse of AUD 2. These signals are applied to the Audio-Regulator H2 and ultimately drive speakers 1 and 2.

AVG0-AVG13
Address bits on Vector-Generator Address Bus lines AVG0-AVG13 are software-generated by Vector Address Controller J1. When VOFF is high, these signals are passed through the Vector Address Selectors on lines AM0-AM13 to the Vector Read-Only Memory and the Vector-Random-Access Memory.

BANK SEL
The Bank Select signal is developed from data on line DB2. When latch RB9 of the Coin Door and Control Panel Output circuit is locked by LATCH, latch RB9 latches the data on DB2 to pin 2 of RB9, producing the BANK SEL signal. BANK SEL is exclusive-Orred with pins A9 of the Coin Door and Control Panel Output circuit to generate the Coin Door Lockout signal.

COIN LOCKOUT
Coin Lockout is a game PCB output signal developed from the data on line DB2. When locked by LATCH, latch RB9 of the Coin Door and Control Panel Output circuit latches the data on DB2 to pin 9 of RB9. From here, the signal is current amplified and inverted by G2 and applied to the Right and Left Lockout Coils of the game Coin Door.

DO-D7
Microprocessor Data Bus lines D0-D7 form a bi-directional data bus between the Microprocessor, the Read-Only Memory, and the Option Switch Input circuit.

D8-D17
Data bits of Y-Axis Vector Data Lines D8-D17 are software-generated by Vector Data Shifters H8, H7, and, by latch of the Op Code and Intensity Latches circuit. D8-D17 and D12 are the input signals for digital-to-analog converter DACS F9 of the Y-Axis Output circuit. The data carried on these lines represents the y-axis signal from the current location of the display beam. If D8-D17 is low, DAC F9 operates only in its lower 512 positions, which means a negative direction of change on the display. D12 is high, DAC F9 operates only in its upper 512 positions for a positive direction of change on the display.

D14-D17 are exclusive-Orred with gate B6 of the Normalization Flag circuit.

DYD0-DYD7
Data bits of Y-Axis Vector Data Lines DYD0-DYD7 are software-generated by Vector Data Shifters H8, H7, and, by latch of the Op Code and Intensity Latches circuit. DYD0-DYD7 and D12 are the input signals for digital-to-analog converter DACS F9 of the Y-Axis Output circuit. The data carried on these lines represents the y-axis signal from the current location of the display beam. If DYD7 is low, DAC F9 operates only in its lower 512 positions, which means a negative direction of change on the display. D12 is high, DAC F9 operates only in its upper 512 positions for a positive direction of change on the display.

DYD7 is applied to latch E8 in the DAC Reference and Bipolar Current Source circuit. These signals together with VCTR and VCTR are set the X REF and Y REF voltage levels via DAC 09.

LINES DYD0-DYD7 carry data representing the eight different color signals for latch K10 of the RGB-R Output circuit.

LINES DYD4-DYD7 carry data representing the intensity signals for latch K10 of the Index/Blanking circuit.

LINES DYD0-DYD10 are latched at 7D of the Vector Scaling circuit. The data carried on these lines represents the number of y-axis (in linear) that the Vector Scaling circuit uses to divide into the vector drawing time. The vector drawing time is divided by 2, where n equals the number represented on DYD0-DYD10.

EARM0
The Electrically-Adjustable ROM Control signal is an active low signal software-generated by Address Decoder P3 at address 8900. EARM0 is the clock signal for latch K2 in the High-Score Table circuit. EARM0 can allow K2 to pass data bits on lines DBO-D13 to the control lines of EARM2.

EARM2
The Electrically-Adjustable ROM Read Enable is an active low signal software-generated by Address Decoder P3 at address 7100. EARM2 is the clock signal for latch K2 in the High-Score Table circuit. EARM2 adds the eight data bits from the game PCB to pass through buffer H2 to the microprocessor data bus.

EARM0W
The Electrically-Adjustable ROM Write Enable is an active low signal software-generated by Address Decoder P3 at address 8940. EARM0W is the clock signal for latches J2 and J2 in the High-Score Table circuit. EARM0W allows address bits on lines A80-A87 and data bits on lines DBO-D10 to pass to the address and data input pins of EAROM M2.
Description of Gravitar PCB Signal Names (continued)

The active low-level Normalization Flag is software-generated by gate K4 of the Normalization Flag circuit. If P0 is high, QA is high, and the output from gate J5 is high, ENORM is set low when STR0ED goes high. ENORM is applied through gate K7 to the S1 input pin of Vector Data Shifters A8, B8, C8, F8, H8, and J8. ENORM multiples the rate of change of data in the Vector Data Shifters via a shift left operation at the same 2nd factor specified by the bit on the Y-Axis Output Circuit. The number is incremented at a 12-MHz rate under both STR0ED and Y-Axis1 changes state, which then sets ENORM to the high level.

The Go flag is an active high-level signal software-generated by gate M5 of the Go Flag circuit when either VCTR or CNTR are high. Go is gated with HALT to gate N5 of the State Machine circuit to produce the A7 input address bit for State Machine ROM #4.

Go is also used as the enable signal for Timer Vector R6. If Go is high, the Timer Vector starts its count. The Timer Vector counts to 256. If 0101P is high and level 1 at low level, and if 051P is low and high is high, the Timer Vector counts to 16K.

The active high-level Haist Flag is software-generated by latch L3 of the Haist Flag circuit. Halt is enabled through buffer M9 of the Coin Door and Control Panel input circuit when STR1P is low to permit Microprocessor C2 to reset the status of Halt on line C9. In addition, HALT is applied to latch P4 of the State Machine circuit to develop HAIST.

Halt is an active high-level Halt Flag is software-generated by latch L3 of the Halt Flag circuit. Halt is enabled through buffer M9 of the Coin Door and Control Panel input circuit when STR1P is low to permit Microprocessor C2 to reset the status of Halt on line C9. In addition, HALT is applied to latch P4 of the State Machine circuit to develop HAIST.

The active low-level Delayed Halt Flag is software-generated by latch L4 of the State Machine circuit. HALT is generated when the Halt signal has been delayed by one pulse of the Inversed VGCK (15 MHz), which in turn has been delayed by one pulse of 12 MHz. HALT is applied with Go by gate N5 of the Inverted VGCK signal to produce the A7 input address bit for State Machine ROM #4.

The active low-level Halt Flag is software-generated by latch L5 of the Halt Flag circuit. Halt is enabled through buffer M9 of the Coin Door and Control Panel input circuit when STR1P is low to permit Microprocessor C2 to reset the status of Halt on line C9. In addition, HALT is applied to latch P4 of the State Machine circuit to develop HAIST.

Interrupt Acknowledge is an active low-level signal software-generated from Address Decoder P3 at address 8800. This signal is an acknowledgment from Microprocessor C2 that a request interrupt has been received. Interrupt resets counter J4.

Invert X is an active high-level signal developed from the data bit on line DB. When high, INVERT X switches data bit D10 through INVERT X to the Coin Door and Control Panel Output circuit which drives the data bit on DB to pin 12 of N6. When high, INVERT X switches data bit D10 through INVERT X to the Coin Door and Control Panel Circuit, which then switches the data bit to the Coin Door and Control Panel Circuit which drives the data bit on DB to pin 12 of N6. When high, INVERT X switches data bit D10 through INVERT X to the Coin Door and Control Panel Circuit, which then switches the data bit to the Coin Door and Control Panel Circuit which drives the data bit on DB to pin 12 of N6. When high, INVERT X switches data bit D10 through INVERT X to the Coin Door and Control Panel Circuit, which then switches the data bit to the Coin Door and Control Panel Circuit which drives the data bit on DB to pin 12 of N6.

Latch 2 is an active low-level signal software-generated by decoder H7 of the State Machine circuit. LATCH is applied through inverter F7 to the 50 input pins of shift register A8, B8, C8, F8, H8, and J8 in the Vector Data Shifters circuit. LATCH causes the data bits on lines D8V1/D8V2 to be latched by A8 and B8 to lines D8V3/D8V4 when A8 is clocked by the 12-MHz clock signal.

Latch 3 is an active low-level signal software-generated by decoder H7 of the State Machine circuit. LATCH is applied through inverter F7 to the 50 input pins of shift register A8, B8, C8, F8, H8, and J8 in the Vector Data Shifters circuit. LATCH causes the data bits on lines D8V1/D8V2 to be latched by A8 and B8 to lines D8V3/D8V4 when A8 is clocked by the 12-MHz clock signal.

LATCH is also the clock signal for Op Code and Intensity Latch D6. When LATCH goes low, the data bits on lines D8V1/D8V2 are latched by C6 to lines D8V1/D8V2 when A8 is clocked by the 12-MHz clock signal.

LATCH also is the clock signal for Op Code and Intensity Latch D6. When LATCH goes low, the data bits on lines D8V1/D8V2 are latched by C6 to lines D8V1/D8V2 when A8 is clocked by the 12-MHz clock signal.

LATCH also is the clock signal for Op Code and Intensity Latch D6. When LATCH goes low, the data bits on lines D8V1/D8V2 are latched by C6 to lines D8V1/D8V2 when A8 is clocked by the 12-MHz clock signal.

The active high-level Normalization Flag is software-generated by latch L5 of the Normalization Flag circuit when P0 is high, ORP is high, and HALT is high. HALT stops the vector clock, and the state of latch L5 determines the direction of data flow through buffer N9.

The active high-level signal software-generated from Address Decoder R2 during addresses 6000 through 6FFF. IO7 is gated with RIBY to gate J6 to produce the direction signal for bidirectional data bus N8 of the Coin Door and Control Panel input circuit. J6 determines the direction of data flow through buffer N9.

The active high-level signal software-generated from Address Decoder R2 at address 6800 through 6FFF. IO7 is used with the ROM signal for gate N4 to enable bidirectional data bus N8 of the Coin Door and Control Panel input circuit. J6 determines the direction of data flow through buffer N9.

The active high-level signal software-generated from Address Decoder R2 at address 6800 through 6FFF. IO7 is used with the ROM signal for gate N4 to enable bidirectional data bus N8 of the Coin Door and Control Panel input circuit. J6 determines the direction of data flow through buffer N9.

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The active high-level signal software-generated from Address Decoder R2 at address 6800 through 6FFF. IO7 is used with the ROM signal for gate N4 to enable bidirectional data bus N8 of the Coin Door and Control Panel input circuit. J6 determines the direction of data flow through buffer N9.

The active high-level signal software-generated from Address Decoder R2 at address 6800 through 6FFF. IO7 is used with the ROM signal for gate N4 to enable bidirectional data bus N8 of the Coin Door and Control Panel input circuit. J6 determines the direction of data flow through buffer N9.

The active high-level signal software-generated from Address Decoder R2 at address 6800 through 6FFF. IO7 is used with the ROM signal for gate N4 to enable bidirectional data bus N8 of the Coin Door and Control Panel input circuit. J6 determines the direction of data flow through buffer N9.

The active high-level signal software-generated from Address Decoder R2 at address 6800 through 6FFF. IO7 is used with the ROM signal for gate N4 to enable bidirectional data bus N8 of the Coin Door and Control Panel input circuit. J6 determines the direction of data flow through buffer N9.

The active high-level signal software-generated from Address Decoder R2 at address 6800 through 6FFF. IO7 is used with the ROM signal for gate N4 to enable bidirectional data bus N8 of the Coin Door and Control Panel input circuit. J6 determines the direction of data flow through buffer N9.

The active high-level signal software-generated from Address Decoder R2 at address 6800 through 6FFF. IO7 is used with the ROM signal for gate N4 to enable bidirectional data bus N8 of the Coin Door and Control Panel input circuit. J6 determines the direction of data flow through buffer N9.

The active high-level signal software-generated from Address Decoder R2 at address 6800 through 6FFF. IO7 is used with the ROM signal for gate N4 to enable bidirectional data bus N8 of the Coin Door and Control Panel input circuit. J6 determines the direction of data flow through buffer N9.

The active high-level signal software-generated from Address Decoder R2 at address 6800 through 6FFF. IO7 is used with the ROM signal for gate N4 to enable bidirectional data bus N8 of the Coin Door and Control Panel input circuit. J6 determines the direction of data flow through buffer N9.

The active high-level signal software-generated from Address Decoder R2 at address 6800 through 6FFF. IO7 is used with the ROM signal for gate N4 to enable bidirectional data bus N8 of the Coin Door and Control Panel input circuit. J6 determines the direction of data flow through buffer N9.

The active high-level signal software-generated from Address Decoder R2 at address 6800 through 6FFF. IO7 is used with the ROM signal for gate N4 to enable bidirectional data bus N8 of the Coin Door and Control Panel input circuit. J6 determines the direction of data flow through buffer N9.

The active high-level signal software-generated from Address Decoder R2 at address 6800 through 6FFF. IO7 is used with the ROM signal for gate N4 to enable bidirectional data bus N8 of the Coin Door and Control Panel input circuit. J6 determines the direction of data flow through buffer N9.

The active high-level signal software-generated from Address Decoder R2 at address 6800 through 6FFF. IO7 is used with the ROM signal for gate N4 to enable bidirectional data bus N8 of the Coin Door and Control Panel input circuit. J6 determines the direction of data flow through buffer N9.
Description of Gravitar PCB Signal Names (continued)

PLAYER 1 LED

The Player 1 LED on signal is developed from the data bit on line DB4. When clocked by LATCH, latch R9 of the Coin Door and Control Panel Output circuit latches the data bit on line DB4 on pin 19 of R9. This signal is applied through R103 to light the Player 1 LED on the game Control Panel.

PLAYER 2 LED

The Player 2 LED on signal is developed from the data bit on line DB5. When clocked by latch R9 of the Coin Door and Control Panel Output circuit latches the data bit on DB5 on pin 16 of R9. This signal is applied through R102 to light the Player 2 LED on the game Control Panel.

POR

The active high-level Power-On Reset signal is hardware-generated at pin 4 of F7 in the Power-On Reset circuit. POR is the clock signal that starts the count of 64 of the Clock circuit.

POR

The active low-level Power-On Reset signal is hardware-generated at pin 6 of Inverter F7 in the Power-On Reset circuit. POR is generated when the voltage pin 3 of R6 is less than about 7 volts or when the RESET test point is shorted to ground. POR is developed into the RESET signal to protect Microprocessor C2.

RAM

The Random-Access Memory Enable is an active low-level signal generated by the Address Decoder R2 during addresses 0000 through 255FF. RAM is the chipenable signal for Random-Access Memory N1P1. When low, RAM allows data to be read from or written to N1P1, depending upon the state of WRITE.

READ

READ is a game PCB output signal developed from the data line D27 at the R4-B Output circuit. When D27V is high and latch K10 is closed by switch K10, the data bit on D27V is inverted and latched to pin 3 of K10. If both BLANK and L6 are low, the data bit is inverted and gated by latch L10 to form K6. Transistor Q6 generates the READ signal for the display data. 

RESET

RESET is an active low-level signal generated at pin 5 of K3 from the Watchdog circuit on the Power-On Reset circuit. The Power-On Reset circuit sets RESET to an active low level whenever the RESSET test point is grounded or during the time that the power-supply voltages are reaching their stabilized, regulated values. This ensures that the Microprocessor Address Bus is stabilized before the microprocessor begins operation.

Watchdog circuit sets RESET to an active low level if the microprocessor fails to output a test waveform before Watchdog counter H4 has reached its maximum count.

RESET is also the clear signal for latch R9 in the Coin Door and Control Panel Output circuit. In addition, RESET is gated with VDD by gate L6 in the Halt Flag circuit to produce HSBIT.

ROM

The Read-Only Memory Enable is an active high-level signal generated from Address Decoder R1 during addresses 0000 through 255FF. ROM1 is OFF when I/O is driven by gate R4 to enable bi-directional data bus buffer F2 to pass data. In addition, ROM is ANDed with DIEQ to enable data buffer E2.

ROM1

Read-Only Memory Chip Select 0 is an active low-level signal generated by the Address Decoder R1 at addresses 0000-1FFF, ROM1 is the chip-select signal for ROM D1 of the Read-Only Memory circuit. When low, ROM1 allows ROM D1 to be addressed and to pass data to buffer E2.

ROM1

Read-Only Memory Chip Select 1 is an active low-level signal generated by the Address Decoder R1 at addresses A000-FFFF. ROM1 is the chip-select signal for ROM E1 of the Read-Only Memory circuit. When low, ROM1 allows ROM E1 to be addressed and to pass data to buffer E2.

ROM2

Read-Only Memory Chip Select 2 is an active low-level signal generated by Address Decoder R1 at addresses 8000-BFFF. ROM2 is the chip-select signal for ROM H1 of the Read-Only Memory circuit. When low, ROM2 allows ROM H1 to be addressed and to pass data to buffer E2.

ROM3

Read-Only Memory Chip Select 3 is an active low-level signal generated by Address Decoder R1 at addresses C000-EFFF. ROM3 is the chip-select signal for ROM J1 of the Read-Only Memory circuit. When low, ROM3 allows ROM J1 to be addressed and to pass data to buffer E2.

ROM4

Read-Only Memory Chip Select 4 is an active low-level signal generated by Address Decoder R1 at addresses 0000-1FFF. ROM4 is the chip-select signal for ROM K1 of the Read-Only Memory circuit. When low, ROM4 allows ROM K1 to be addressed and to pass data to buffer E2.

ROM5

Read-Only Memory Chip Select 5 is an active low-level signal generated by Address Decoder R1 at addresses 8000-FFFF. ROM5 is the chip-select signal for ROM M1 of the Read-Only Memory circuit. When low, ROM5 allows ROM M1 to be addressed and to pass data to buffer E2.

R/W

The Buffered Read/Write Enable is generated by Microprocessor C2, buffered by B1, and applied to the read/write enable signal for custom audio chips B3 and C/D of the Option Switch Input and Audio Output circuit. In the high state, R/W is high. R/W is the enable for the custom audio chips; in the low state, it is the write enable for these chips.

R/W

The Buffered Read/Write Enable is generated at pin 2 of F3 in the Microprocessor circuit by inverting R/WB. R/WB is ANDed with holding B2 and 3 MHz by gate K4 to produce WRITE, R/WB is the direction signal for Memory Data Buffer P8 and determines the direction of data flow through P8. In the high state, R/WB allows data to pass through P8 from the data bus to the vector generator data bus; in the low state, it allows data to pass in the reverse direction.

SA

The active high-level Signature Anchor Flag is hardware-generated at pin 15 of inverter J2 when test point SA at pin 13 is grounded. SA is used to place the game PCB in the mode to generate signatures for reading by a Signature Analyzer or the ATARI CAT Box.

SACLK

Signature Anchor Clock is a test point at pin 8 of gate G7 in the State Machine Clock Logic circuit. SACLK is used to apply the clock signal from the Signature Analyzer or ATARI CAT Box for the reading of game PCB signatures.

SAEN

Signature Enable is a test point at pin 8 of gate G5 in the Vector Address Selector circuit. SAEN is generated by gating VRAM with the data bit on line AM10 by gates J2 and M5. SAEN is used to enable a Signature Analyzer or the ATARI CAT Box for reading of game PCB signatures.

NClk

NClk is an active high-level signal generated by the Gate B of the Vector Scaling circuit. When OP2 is high and control C7 is counting down, SCALE is gated with NClk at gate K5 of the Vector Timer circuit to produce the load signal for Vector Timers M5, M6, M, and R6. When SCALE is high, the Vector Timers perform a load operation for each count of C7 at a 12-NHz rate. This results in a vector drawing time divided by a factor of 27, n equals the total counts of C7. When SCALE reaches its minimum count, SCALE is set low.

NClk is gated with VCIR, CNTN, DVY11-DVY12, and DVY11-DVY12 of the Normalization Flag circuit to produce the clear signal for latch A6.

SCALE

Scale Load is an active low-level signal generated by gates N3, L3, and L6 of the Vector Generator circuit. When STROBE2, OP2, and DVY12 are all low, SCALE is set to low. SCALE is the clock signal for Vector Scaling latch D7. When SCALE is high, the data on lines DVY11-DVY12 are latched to the output pins.

SINP1

Switch Input 1 is an active low-level signal generated by Address Decoder R2 at address 0000. SINP1 is the direction signal for bi-directional data buffer M1 of the Coin Door and Control Panel Input circuit and determines the direction of data flow through data bus buffer M6.

SINP2

Switch Input 2 is an active low-level signal generated by Address Decoder R2 at address 8000. SINP2 is the direction signal for bi-directional data buffer L3 of the Coin Door and Control Panel Input circuit and determines the direction of data flow through data bus buffer L6.

STATCLK

State Clock is an active low-level signal generated by switches J3 and L6 of the Vector Generator circuit. When STROBE2, OP2, and DVY12 are all low, STATCLK is set low. STATCLK is the clock for latch K9 in the R-G-B Output circuit and latch E8 in the I-Intensity and Blanking circuit. When STATCLK goes high, the data bits on DVY9-DVY12 are latched by K10, and those on DVY14-DVY7 are latched by E8.

STOP

Stop is an active low-level signal generated by gate H3 of the Vector Timer circuit. STOP is set low when Vector Timers N6, M6, M, and R6 have reached their maximum count. STOP is low when VCIR from Vector Flag latch E5 and CNTN from Center Flag latch B5 is set low when E5 is clocked by the 12-NHz clock signal.

STROBE1

Strobe 0 is an active low-level signal generated by State Machine decoder H7. STROBE1 is the signal for Normalization Flag latch A8. It is also the STROBE input for Vector Address Controller J9.

STROBE2

Strobe 2 is an active low-level signal generated by State Machine decoder H7. If OP2 is low, when STROBE goes low, the data latched at the outputs of D7 in the Vector Scaling circuit are latched into counter C7. When STROBE goes high, C7 begins counting down.

STROBE1 is the STROBE input for Vector Address Controller J9.

STROBE2

Strobe 2 is an active low-level signal generated by State Machine decoder H7. If OP2 and DVY12 are both low, SCALE and DVY11 are both low STROBE2 goes low if OP2 and DVY12 are both low. STROBE2 is set low when STROBE goes low.

STROBE2 is the STROBE input for Vector Address Controller J9.

STROBE3

Strobe 3 is an active low-level signal generated by State Machine decoder H7. STROBE3 is the clock signal for Halt Flag latch L5 and is the STROBE input for Vector Address Controller J9.

STROBE3

Strobe 3 is the clock signal for Halt Flag latch L5 and STROBE3 is the STROBE input for Vector Address Controller J9.
Description of Gravitar PCB Signal Names (continued)

STATE

ST3

State signal ST3 is an active high-level signal hardware-generated by Decoder Disable latch A7. ST3 is opposite in state to VGCK, and is delayed by one pulse of the 12MHz clock signal if the 04 output from State Machine RDM 4 is low and VEMEM is high. If the 04 output from 16 is high, ST3 is high. When ST3 is low, 04ST2 and the data on lines ST0-ST2 to put LATCH0-LATCH2 and STROBE0-STROBE3.

VCVR, VCTR

The Vector Signal latches are software-generated by Vector Flag latch 05, 06, 07, 08, STROBE, and VCTR and VCR are low and are not high, VCVR is set high and VCTR is set low when EI is clocked by the 12MHz clock signal. VCVR is held with 0N by gate M5 to set GO high.

SCALE, CNTR, D1V41, D1V2, and D1V4 are gated with VCVR to produce the clear signal for Nominal Flag latch A8.

In the Z Intensity and Blanking circuit, VCTR is the clock signal for latch 06 and the serial input signal for switch register M3.

VCVR and VCR are used by the DAC Reference and Bipolar Current Sources circuit to set the X BIP, Y BIP, X REF, and Y REF levels.

VGCK

The Vector Generator clock signal is generated at pin 18 of buffer B1 in the Microprocessor circuit. VGCK is derived from the 1.5 MHz clock signal and is applied to AND gate 05 of the State Machine Clock Circuit. VGCK is the basic timing signal of the State Machine circuit.

VGGO

The Vector Generator Go signal is an active low-level signal software-generated by Address Decoder D0 at address 8840. VGGO is the clear signal for latch 05 of the Half Flag circuit. When low, VGGO sets HALT to the inactive low level.

VGCRST

Vector Generator Reset is an active low-level signal software-generated by Address Decoder D0 at address 8890. VGCRST is ORed with gate b4 of the Half-Flag circuit to produce DISRG.

VEMEM

The Vector Memory Select Enable is an active low-level signal software-generated by Address Decoder D0 at address 8200 through 82FF. VEMEM is the select-enable signal for Vector Address Selectors K5, K6, M4, and M6. When low, VEMEM allows the Vector Address Selectors to produce VV, BUFFER, and the AM0-AM12 multiplexed address bits. VEMEM is also applied to gate K5 of the Vector State Machine Clock Circuit which it is used to generate ST3.

VRAM

The Vector Random-Access Memory Chip Enable is an active low-level signal software-generated by Address Decoder D0 at addresses 2000-27FF. When low, VRAM enables Vector Random-Access Memory K7 to be addressed to both receive or transmit data, depending upon the state of VV. VRAM is also used to produce the DAE signal from M5 of the Vector Address Selector circuit.

VRDO0

Vector Read-Only Memory Chip Select 0 is an active low-level signal software-generated by Vector Address Decoder D0 at addresses 2000-27FF. VRDO0 is the chip-select signal for ROM L7 of the Vector Read-Only Memory circuit. When low, VRDO0 allows ROM L7 to be addressed and to pass data to the Vector Generator Data Bus.

VRDO1

Vector Read-Only Memory Chip Select 1 is an active low-level signal software-generated by Vector Address Decoder D1 at addresses 3000-37FF. VRDO1 is the chip-select signal for ROM M/N7 of the Vector Read-Only Memory circuit. When low, VRDO1 allows ROM M/N7 to be addressed and to pass data to the Vector Generator Data Bus.

VRDO2

Vector Read-Only Memory Chip Select 2 is an active low-level signal software-generated by Vector Address Decoder D2 at addresses 4000-47FF. VRDO2 is the chip-select signal for ROM N/P7 of the Vector Read-Only Memory circuit. When low, VRDO2 allows ROM N/P7 to be addressed and to pass data to the Vector Generator Data Bus.

VRDO3

Vector Read-Only Memory Chip Select 3 is an active low-level signal software-generated by Vector Address Decoder D3 at addresses 5000-57FF. VRDO3 is the chip-select signal for ROM R7 of the Vector Read-Only Memory circuit. When low, VRDO3 allows ROM R7 to be addressed and to pass data to the Vector Generator Data Bus.

WWW

The Vector Write Enable is an active low-level signal software-generated by Vector Address Selector K8, ANDed with gate C6, and applied as the write-enable signal for Vector Random-Access Memory K7. When low, WWW allows data to be written to K7, when high, WWW permits data to be read from K7.

WDCR

Watching Clear is an active low-level signal software-generated by Address Decoder D3 at address 8890. WDCR is ORed with PDR by gate E3 to clear the count of Watching counter H4.

WWDS

Watching Disable is a test point at pin 9 of AND gate L4 in the Watching circuit. When WWDS is grounded, RESET is prevented from going to an active low level (except when the RESET test point is grounded).

WRITE

Write Enable is an active low-level signal generated by gate K4 of the Microprocessor circuit. WRITE is used to enable Address Decoder D0 and Random-Access Memory K7. WRITE is also applied to pin 11 of K8 in the Vector Address Selector circuit to develop VV.

X BIP

The X-Axis Bipolar Current is set by R96 of the DAC Reference and Bipolar Current Sources circuit. This is the current source for pins 18 of 4x4 digital-to-analog converter (DAC) A/B8 of the X-Axis Output circuit.

X OUT

X Output is a game PCB output signal generated by the X-Axis Output circuit. X OUT carries the horizontal beam deflection signal for the drawing of vectors on the display.

X REF

The X-Axis Voltage Reference is set by DAC Reference and Bipolar Current Sources circuit. This is the reference voltage applied to pin 14 of 4x4 digital-to-analog converter (DAC) A/B8 of the X-Axis Output circuit.

Y BIP

The Y-Axis Bipolar Current is set by R96 of the DAC Reference and Bipolar Current Sources circuit. This is the current source for pin 18 of 4x4 digital-to-analog converter (DAC) F9 of the Y-Axis Output circuit.

Y OUT

Y Output is a game PCB output signal generated by the Y-Axis Output circuit. Y OUT carries the vertical beam deflection signal for the drawing of vectors on the display.

Y REF

The Y-Axis Voltage Reference is set by the DAC Reference and Bipolar Current Sources circuit. This is the reference voltage applied to pin 14 of 4x4 digital-to-analog converter (DAC) F9 of the Y-Axis Output circuit.

Z BIP, Z VS

Z Intensity signals Z022 and ZZ12 are software-generated by latch C8 in the Op Code and Intensity Latches circuit. These signals are delivered from the data on lines D2V12-D2V7 when C6 is clocked by LATCH0. If the binary count carried by 022 is not equal to 1, these signals are the input signals for latch F6 in the Z Intensity and Blanking circuit. If the binary count carried by 022 is 1, Z Intensity signals ZZ12, ZZ22, and ZZ32 are ANDed by gate F5 of the Z Intensity and Blankling circuit to produce the select signal for latch F6. This select signal causes the latched data from E8 to be applied as the input signals for latch F6.

Z OUT

Z Intensity Output is a game PCB output signal generated by the Z Intensity and Blankning circuit from either D2V41-D2V7 or 022. The Z output signals from latch F6 are summed at the base of Q7. Transistors Q7 and Q8 buffer Z OUT before it is sent to the game display circuitry to control the display intensity.

3 KHZ

The 3 kHz clock signal is generated at pin 6 of Clock counter F4 and is applied through switch input buffer M9 of the Coin-Door and Control Panel Input circuit (when SN10 is low). The 3 kHz clock is read by the microprocessor on data line D87. This frequency is the time reference for the Microprocessor C2.

12 KHZ

The 12 kHz clock signal is generated at pin 4 of Clock counter F4 and is applied to reset A4 of the High-Score Table.

6 MHz

The 6 MHz clock signal is generated at pin 3 of Clock counter F4 and is applied to gate J5 of the State Machine Clock Circuit.

12 MHz

The 12 MHz clock signal is generated at pin 10 of inverter F3 in the Clock circuit. This signal clocks the Vector Timer Shifters, the Vector Flag latch, and the Center Flag latch.
Troubleshooting with the Read/Write Controller

A. CAT Box Preliminary Set-Up

1. Remove the electrical power from the game.
2. Remove the wiring harness from the game PCB.
3. Remove the game PCB from the game cabinet.
4. Remove Microprocessor C2 from the game PCB.
5. Connect the harness from the game to the game PCB (Use extend cables, if available.)
6. Connect together the 40 and 42 test points on the game PCB with the shortest possible jumper.
7. Connect the WDDS test point to ground.
8. Connect the CAT Box flex cable to the game PCB edge test connector.
9. Apply power to the game and to the CAT Box.
10. Set CAT Box switches as indicated:
   a. TESTER SELF-TEST: OFF
   b. TESTER MODE: R/W
   c. TESTER 11: OFF
11. Press TESTER RESET.

B. Address Lines

1. Perform the CAT Box preliminary set-up.
2. Connect the DATA PROBE to the CAT Box.
3. Connect the DATA PROBE ground clip to a game PCB ground test point.
4. Set CAT Box switches as indicated:
   a. BYTES: 1
   b. PULSE MODE: UNLATCHED
   c. R/W MODE: OFF
   d. R/W: WRITE
5. Key in the address pattern given in Table 1 (use A to start) with the CAT Box keyboard.
6. Press DATA SET.
7. Key in the pattern given in Table 1 (use A to start) with the CAT Box keyboard.
8. Set R/W MODE: STATIC.
9. Probe the IC-pin with the DATA PROBE and check that the 1 or 0 LED indicated in Table 2 lights up. Repeat this step for each IC-pin in Table 2.
10. Repeat parts 6 through 9 using data 555 in part 7.

D. RAM

1. Perform the CAT Box preliminary set-up.
2. Set CAT Box switches as indicated:
   a. DBUS SOURCE: ADDR
   b. BYTES: 1024
   c. R/W: OFF
   d. R/W: WRITE
3. Enter address 0000 with the keyboard.
4. Set R/W MODE to PULSE and back to (OFF).
5. Set R/W: READ.
6. Set R/W MODE to PULSE and back to (OFF).
7. If the CAT Box reads an address that doesn't compare with that written, the COMPARE ERROR LED will light up. The ADDRESS/SIGNATURE display of the CAT Box will show the failing address location and the ERROR DATA DISPLAY switch is enabled.

---

Table 1 Address Lines

<table>
<thead>
<tr>
<th>LOGIC STATE</th>
<th>IC-PIN</th>
<th>LOGIC STATE</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>R2-12</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>R2-13</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>R2-14</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>B1-5</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>B1-7</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>B1-12</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>B1-14</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>B1-16</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>C1-9</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>C1-17</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>C1-15</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>C1-12</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>C1-14</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>C1-16</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>C1-18</td>
<td>1</td>
</tr>
</tbody>
</table>

---

Table 2 Address BUS

<table>
<thead>
<tr>
<th>ADDRESS BUS</th>
<th>DATA BUS</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>A15 A14 A13</td>
<td>A12 A11 A10 A9</td>
<td>A8 A7 A6 A5 A4 A3 A2 A1</td>
</tr>
<tr>
<td>D7 D6 D5 D4</td>
<td>D3 D2 D1 D0</td>
<td>R/W</td>
</tr>
</tbody>
</table>

---

Memory Map

<table>
<thead>
<tr>
<th>ADDRESS</th>
<th>CONTENT</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000-0FFF</td>
<td>E0000</td>
</tr>
<tr>
<td>0100-01FF</td>
<td>E0100</td>
</tr>
<tr>
<td>0200-02FF</td>
<td>E0200</td>
</tr>
<tr>
<td>0300-03FF</td>
<td>E0300</td>
</tr>
<tr>
<td>0400-04FF</td>
<td>E0400</td>
</tr>
<tr>
<td>0500-05FF</td>
<td>E0500</td>
</tr>
<tr>
<td>0600-06FF</td>
<td>E0600</td>
</tr>
<tr>
<td>0700-07FF</td>
<td>E0700</td>
</tr>
<tr>
<td>0800-08FF</td>
<td>E0800</td>
</tr>
<tr>
<td>0900-09FF</td>
<td>E0900</td>
</tr>
<tr>
<td>0A00-0AFF</td>
<td>E0A0</td>
</tr>
<tr>
<td>0B00-0BFF</td>
<td>E0B0</td>
</tr>
<tr>
<td>0C00-0CFF</td>
<td>E0C0</td>
</tr>
<tr>
<td>0D00-0DFF</td>
<td>E0D0</td>
</tr>
<tr>
<td>0E00-0EFF</td>
<td>E0E0</td>
</tr>
<tr>
<td>0F00-0FFF</td>
<td>E0F0</td>
</tr>
</tbody>
</table>

---

Graviton™ PCB Troubleshooting

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Interlink Communications Company

SP-206 Sheet 11A
1st printing
ed. Using this switch, determine if the error is in the high-order or low-order RAM.
8. Repeat parts 2-7 through 7 using addresses 0400, 2000, and 2400.
9. Repeat this test with DBUS SOURCE set to ADDR.

E. Custom Audio I/O Chips

Gravitar has two custom audio I/O chips. Each must be tested separately. There are several ways to test these chips:

- Perform the self-test.
- Substitute a known good part for a suspected defective part.
- Use the following procedure.

1. Perform the CAT Box preliminary set-up.

Table 2 Data Lines

<table>
<thead>
<tr>
<th>When writing</th>
<th>Data lines</th>
<th>When writing</th>
<th>55 pattern</th>
</tr>
</thead>
<tbody>
<tr>
<td>AA pattern</td>
<td>IC-PIN</td>
<td>LOGIC STATE</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>F2-11</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>F2-12</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>F2-13</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>F2-14</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>F2-15</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>F2-16</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>F2-17</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>F2-18</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>F2-9</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>F2-8</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>F2-7</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>F2-6</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>F2-5</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>F2-4</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>F2-3</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>F2-2</td>
<td>1</td>
<td></td>
</tr>
</tbody>
</table>

2. Set CAT Box switches as indicated:
   a. BYTES: 1
   b. R/W: WRITE
   c. R/W MODE: (OFF)
3. Enter the address from Table 3 with the keyboard.
4. Press DATA SET.
5. Enter the data from Table 3 with the keyboard.
6. Set R/W MODE to PULSE and back to (OFF).
7. Repeat parts 3 through 6 for each address and data listed in Table 3. Check for the response indicated.

Table 3 Custom Audio I/O Chips

<table>
<thead>
<tr>
<th>ADDRESS</th>
<th>DATA</th>
<th>TEST RESULTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>6800</td>
<td>00</td>
<td>Custom Audio I/O Chip B3 channel 1 produces pure tone.</td>
</tr>
<tr>
<td>6801</td>
<td>00</td>
<td>Custom Audio I/O Chip B3 channel 1 off.</td>
</tr>
<tr>
<td>6802</td>
<td>55</td>
<td>Custom Audio I/O Chip B3 channel 2 produces pure tone.</td>
</tr>
<tr>
<td>6803</td>
<td>55</td>
<td>Custom Audio I/O Chip B3 channel 2 off.</td>
</tr>
<tr>
<td>6804</td>
<td>00</td>
<td>Custom Audio I/O Chip C3 channel 1 produces pure tone.</td>
</tr>
<tr>
<td>6805</td>
<td>00</td>
<td>Custom Audio I/O Chip C3 channel 1 off.</td>
</tr>
<tr>
<td>6806</td>
<td>55</td>
<td>Custom Audio I/O Chip C3 channel 2 produces pure tone.</td>
</tr>
<tr>
<td>6807</td>
<td>55</td>
<td>Custom Audio I/O Chip C3 channel 2 off.</td>
</tr>
</tbody>
</table>

F. Player and Option Switch Inputs

1. Perform the CAT Box preliminary set-up.
2. Set CAT Box switches as indicated:
   a. BYTES: 1
   b. R/W: READ
3. For each address listed in Table 4, do the following:
   a. Set R/W MODE to (OFF).
   b. Enter the address with the keyboard.
   c. Set R/W MODE to STATIC.
   d. Activate the input switch indicated in Table 4 for the address.

Table 4 Player and DIP Switch Inputs

<table>
<thead>
<tr>
<th>ADDRESS</th>
<th>INPUT SWITCH</th>
<th>TEST RESULTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>7800</td>
<td>Right coin switch, Left coin switch, Self-test switch</td>
<td>Lower nybble (right digit) of DATA display changes when right or left coin, or self-test switches are activated. Upper nybble of DATA display is unstable.</td>
</tr>
<tr>
<td>8000</td>
<td>Player 1 SHIELDS, FIRE, ROTATE LEFT, ROTATE RIGHT, THRUST, START</td>
<td>Upper nybble of DATA display changes when each input switch is activated.</td>
</tr>
<tr>
<td>8800</td>
<td>Player 2 SHIELDS, FIRE, ROTATE LEFT, ROTATE RIGHT, THRUST, START</td>
<td>Upper nybble of DATA display changes when each input switch is activated.</td>
</tr>
</tbody>
</table>

G. Analog Vector-Generator

1. Perform the CAT Box preliminary set-up.
2. Set CAT Box switches as indicated:
   a. DBUS SOURCE: DATA
   b. R/W: WRITE
   c. R/W MODE: (OFF)
3. Enter address 2000 with the keyboard.
4. Press DATA SET.
5. Enter the data from Table 5.
6. Set R/W MODE to PULSE and back to (OFF).
7. Repeat parts 4 through 6 for each address listed in Table 5 using the ADDRESS INCR button to advance the address by 1.

CAUTION

You may damage the circuitry of the X-Y display if you key in the VGOO signal without first checking all the addresses and data. Check the data by reading each address location using parts 8 through 11 below.

8. Set CAT Box switches as indicated:
   a. R/W: READ
   b. R/W MODE: (OFF)
9. Enter address or press ADDRESS INCR.
10. Set R/W MODE to PULSE.
11. Check the data shown in the DATA display against that listed in Table 5. If the data is correct, proceed with part 12.
12. Set CAT Box switches as indicated:
   a. R/W: WRITE
   b. R/W MODE: (OFF)

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SP-206 Sheet 11B
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13. Enter VGO address 8840.
14. Set R/W MODE to PULSE and back to (OFF).
15. Check that the screen shows a large plus sign. Failure of the horizontal or vertical circuits shows up as a single line drawn on the screen. If the screen does not display a large plus sign, contact Atari Field Service.

### Table 5 Analog Vector-Generator Data

<table>
<thead>
<tr>
<th>ADDRESS</th>
<th>DATA</th>
<th>DATA</th>
<th>DATA</th>
</tr>
</thead>
<tbody>
<tr>
<td>2000</td>
<td>00</td>
<td>2000</td>
<td>00</td>
</tr>
<tr>
<td>2001</td>
<td>70</td>
<td>2000</td>
<td>21</td>
</tr>
<tr>
<td>2002</td>
<td>40</td>
<td>2000</td>
<td>80</td>
</tr>
<tr>
<td>2003</td>
<td>80</td>
<td>200F</td>
<td>1F</td>
</tr>
<tr>
<td>2004</td>
<td>77</td>
<td>2010</td>
<td>80</td>
</tr>
<tr>
<td>2005</td>
<td>64</td>
<td>2011</td>
<td>1F</td>
</tr>
<tr>
<td>2006</td>
<td>00</td>
<td>2012</td>
<td>00</td>
</tr>
<tr>
<td>2007</td>
<td>00</td>
<td>2013</td>
<td>01</td>
</tr>
<tr>
<td>2008</td>
<td>80</td>
<td>2014</td>
<td>00</td>
</tr>
<tr>
<td>2009</td>
<td>1F</td>
<td>2015</td>
<td>20</td>
</tr>
<tr>
<td>200A</td>
<td>00</td>
<td>2016</td>
<td>00</td>
</tr>
<tr>
<td>200B</td>
<td>00</td>
<td>2017</td>
<td>E0</td>
</tr>
</tbody>
</table>

### Table 6 LED and Coin Counter Outputs

<table>
<thead>
<tr>
<th>ADDRESS</th>
<th>DATA</th>
<th>DATA</th>
<th>DATA</th>
</tr>
</thead>
<tbody>
<tr>
<td>2000</td>
<td>00</td>
<td>2000</td>
<td>00</td>
</tr>
<tr>
<td>2001</td>
<td>70</td>
<td>2000</td>
<td>21</td>
</tr>
<tr>
<td>2002</td>
<td>40</td>
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</tr>
<tr>
<td>2003</td>
<td>80</td>
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<td>1F</td>
</tr>
<tr>
<td>2004</td>
<td>77</td>
<td>2010</td>
<td>80</td>
</tr>
<tr>
<td>2005</td>
<td>64</td>
<td>2011</td>
<td>1F</td>
</tr>
<tr>
<td>2006</td>
<td>00</td>
<td>2012</td>
<td>00</td>
</tr>
<tr>
<td>2007</td>
<td>00</td>
<td>2013</td>
<td>01</td>
</tr>
<tr>
<td>2008</td>
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<td>2014</td>
<td>00</td>
</tr>
<tr>
<td>2009</td>
<td>1F</td>
<td>2015</td>
<td>20</td>
</tr>
<tr>
<td>200A</td>
<td>00</td>
<td>2016</td>
<td>00</td>
</tr>
<tr>
<td>200B</td>
<td>00</td>
<td>2017</td>
<td>E0</td>
</tr>
</tbody>
</table>

### Table 7 Address Bus Signatures

<table>
<thead>
<tr>
<th>IC-PIN</th>
<th>SIGNAL NAME</th>
<th>SIGNATURE</th>
</tr>
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<tbody>
<tr>
<td>C1-18</td>
<td>AB0</td>
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<td>C1-16</td>
<td>AB1</td>
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<td>AB2</td>
<td>CCC</td>
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<td>AB3</td>
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<td>C1-8</td>
<td>AB5</td>
<td>0AF</td>
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<td>C1-6</td>
<td>AB6</td>
<td>UPPH</td>
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<td>AB8</td>
<td>HCB8</td>
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<td>B1-14</td>
<td>AB9</td>
<td>2H70</td>
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<td>B1-12</td>
<td>AB10</td>
<td>HPPO</td>
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<td>AB11</td>
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<td>AB12</td>
<td>HAP7</td>
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<tr>
<td>R2-14</td>
<td>A15</td>
<td>755U</td>
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### Troubleshooting with Signature Analysis

#### A. Signature Analysis Setup

1. Perform the CAT Box preliminary set-up.
2. Connect the three BNC-to-EZ clip cables supplied with CAT Box to the SIGNATURE ANALYSIS CONTROL, START, STOP, and CLOCK jacks of the CAT Box.
3. Connect the three black EZ clips to a game PCB ground test point.
4. Connect the CAT Box DATA PROBE to the DATA jack on the CAT Box.
5. Set the CAT Box switches as indicated:
   a. TESTER MODE: SIG
e. TESTER SELF-TEST: OFF
c. PULSE MODE: LATCHED
d. START: Negative-going edge trigger
e. STOP: Negative-going edge trigger
f. CLOCK: Negative-going edge trigger

#### B. Address Lines

1. Perform the signature analysis set-up.
2. Connect the START probe tip to pin 14 of IC R2.
3. Connect the STOP probe tip to pin 14 of IC R2.
4. Connect the CLOCK probe tip to 42 test point on the game PCB.
5. Verify the set-up connections by connecting the DATA PROBE to a game PCB ground test point. The CAT BOX ADDRESS/SIGNATURE display should show 0000. Now connect the DATA PROBE to a +5V test point; the ADDRESS/SIGNATURE display should show 0001.

#### C. Address Decoder

**CAUTION**

While testing decoders and ROMs, adding 270 pF capacitors to A12, A13, A14, and A15 may be necessary to eliminate unstable signatures.

1. Perform parts 1 through 5 of the address bus signature procedure.
2. Probe the IC-PIN listed in Table 8 with the DATA PROBE and check for the signature indicated. Repeat this check for each IC-PIN listed.

### Table 8 Decoder Signatures

<table>
<thead>
<tr>
<th>IC-PIN</th>
<th>SIGNAL NAME</th>
<th>SIGNATURE</th>
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</thead>
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<tr>
<td>R2-1</td>
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<td>R2-4</td>
<td>BD2</td>
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<td>BD3</td>
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<td>R2-6</td>
<td>BD4</td>
<td>942F</td>
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<td>R2-7</td>
<td>BD5</td>
<td>3PCF</td>
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<td>R2-8</td>
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<td>94AF</td>
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<td>3AF</td>
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<td>ROM14</td>
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<td>ROM56</td>
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</tbody>
</table>

### Watchdog Troubleshooting

The Watchdog circuit will send continuous reset pulses to the microprocessor if a problem exists within the microprocessor circuit. If the self-test fails to run, it is a good practice to check the reset line. RESET is a microprocessor input (pin 40). In a properly operating game, reset should occur during power-up or when the RESET test point is grounded. A pulsing RESET line indicates that something is causing the microprocessor to lose its place in the program. Typical causes are:

- Open or shorted address or data bus lines.
- Bad microprocessor chip.
- Bad bus buffers.
- Bad ROM.
- Bad RAM.
- Any bad input or output that causes an address or data line to be held in a constant high or low state.

A pulsing RESET signal indicates a problem exists somewhere within the microprocessor circuitry rather than within the analog vector-generator.

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**CAUTION**

If you write ON data to activate a solenoid, deactivate the solenoid immediately by writing the OFF data. If you leave a solenoid activated for more than 10 seconds, you may have to replace the solenoid and/or its driver, due to overheating.

4. For each DATA output listed in Table 5, do the following:
   a. To activate the output:
      i. Press DATA SET.
      ii. Enter the ON data listed for the output.
      iii. Set R/W MODE to STATIC and back to (OFF).
   b. To deactivate the output:
      i. Press DATA SET.
      ii. Enter the OFF data listed for the output.
      iii. Set R/W MODE to STATIC and back to (OFF).